volume until the size of said semiconductor unit meets an expected specification.

11. (Amended) A method for reducing the size of at least a semiconductor unit in a process of lead-on-chip packaging wherein said semiconductor unit includes a first surface and a second surface, said first surface having at least an electrical connection device thereon, said second surface having no electrical connection device thereon, said method comprising:

attaching said semiconductor unit to a chip carrier in such a way that said semiconductor unit and said chip carrier are in a configuration of lead-on-chip, with said first surface facing said chip carrier and said second surface exposed; and

etching said semiconductor unit from said second surface to reduce semiconductor unit volume until the size of said semiconductor unit meets an expected specification.

19. (Amended) A method for reducing the size of at least a semiconductor unit in a process of packaging said semiconductor unit wherein said semiconductor unit includes a first surface and a second surface, said first surface having at least an electrical connection device thereon, said second surface having no electrical connection device thereon, said method comprising:

dividing a wafer into a plurality of dice;

placing at least one die of said dice onto a seating apparatus, with said second surface exposed;

applying beams of light on said second surface to reduce die volume, with said first surface shielded by said seating apparatus from said beams of light.